

Declaration page 1 of 2  
10/631,328

DOCKET NO. 00-253/1D  
81605(6653)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): NAGARAJAN, Kumar  
et al.  
Serial No.: 10/631,328  
Filed: July 30, 2003  
For: BALANCED COEFFICIENT OF  
EXPANSION FOR FLIP CHIP  
BALL GRID ARRAY  
Art Unit: 2824  
Examiner: Smith, Bradley K.

CERTIFICATE OF TRANSMISSION/MAILING

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VA 22313-1450 on the date below.

June 23, 2004

Rhonda L. Mason

DECLARATION UNDER 37 C.F.R. § 1.131

We, KUMAR NAGARAJAN, ZAFER KUTLU and SHIRISH SHAH,  
hereby declare as follows:

1. We are the co-inventors of the invention disclosed  
and claimed in the subject application, which is a divisional  
of Serial No. 09/680,759, now U.S. Patent 6,639,321 B1;

2. We submitted a copy of the invention disclosure  
attached hereto for "CTE BALANCED FLIP CHIP BGA" to LSI Logic  
Corporation before the filing date of August 30, 2000, of U.S.  
Patent 6,441,499 B1 by Nagarajan, et al.;

3. We conceived the invention disclosed in the

Declaration page 2 of  
10/631,328

DOCKET NO. 00-253/1D  
81605(6653)

attached invention disclosure in the United States of  
America;

4. The undersigned further declare that all statements  
made herein of our own knowledge are true; and that all  
statements not based on our own knowledge are believed to be  
true; and further that these statements were made with the  
knowledge that willful false statements are punishable by  
fine or imprisonment, or both, under Section 1001 of Title  
18 of  
the United States Code.

/s/ [Signature]  
DATE 5/24/04 SIGNATURE  
KUMAR NAGARAJAN

/s/ \_\_\_\_\_  
DATE \_\_\_\_\_ SIGNATURE  
ZAFER KUTLU

/s/ \_\_\_\_\_  
DATE \_\_\_\_\_ SIGNATURE  
SHIRISH SHAH

Declaration page 1 of 2  
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\_\_\_\_\_  
/s/

DATE

SIGNATURE

KUMAR NAGARAJAN

\_\_\_\_\_  
/s/

DATE

SIGNATURE

5/25/04

ZAFER KUTLU

\_\_\_\_\_  
/s/

DATE

SIGNATURE

5/25/04

SHIRISH SHAW

| LSI LOGIC - INVENTOR ON DISCLOSURE FORM                                   |   | Disclosure No. P- 00253                                     |
|---|---|---|
| 1. INVENTOR(S)  |   |   |
| A.  | NAME: Kumar Nagarajan<br>HOME ADDRESS: 1448 Birchmeadow Lane, San Jose, CA - 95131<br>M/S - F124  | EXT. 7317<br>HOME PHONE: 408-428-0883<br>CITIZENSHIP: India |
| B.  | NAME: Zafer Kutlu<br>HOME ADDRESS: 1230 Middle Ave., Menlo Park, CA 94305<br>M/S - F124   | EXT. 7020<br>HOME PHONE: 650-322-7545<br>Citizenship: USA   |
| C.  | NAME: Shirish Shah<br>HOME ADDRESS: 5727 Oleander Common, Fremont, CA 94555<br>M/S - F124   | EXT: 8331<br>Home Phone: 510-494-0886<br>CITIZENSHIP: India |
| D.  | DIVISION, DEPARTMENT, SUBSIDIARY: ADVANCED PROCESS DEVELOPMENT<br>DIRECTOR: John McCormick / Ed Fulcher<br>VICE PRESIDENT: Maniam Alagaratnam |   |
| 2. TITLE OF THE INVENTION (MUST BE Filled OUT) CTE Balanced Flip Chip BGA |   |   |
| 3. CONCEPTION OF THE INVENTION  |   |   |
| A.  | DATE OF FIRST DRAWING   | 3/18/00   |
|   | WHERE CAN FIRST DRAWING BE FOUND?   | Enggr   |
| B.  | DATE OF FIRST WRITTEN DESCRIPTION   | 3/18/00   |
|   | WHERE IS DESCRIPTION FOUND?   |   |
| C.  | DATE OF FIRST ORAL DISCLOSURE TO OTHERS   | 3/15/00   |
|   | TO WHOM?  |   |
| 4. CONSTRUCTION OF DEVICE   |   |   |
| A.  | DATE COMPLETED  | 3/18/00   |
| B.  | WAS PROTOTYPE MADE?   | No  |
| C.  | BY WHOM MADE?   |   |

INVENTORS:

RECEIVED

MAY 03 2000

LSI LOGIC CORP.  
INTELLECTUAL PROPERTY DEPT.

LSI LOGIC

4/28/00  
Zafer S. Kutlu  
Shirish Shah  
DATE 4/29/00  
DATE 4/28/00

WITNESS, READ AND UNDERSTOOD BY:

(PRINT) Kishore V. Desai (SIGN) [Signature] DATE 5/11/00  
(PRINT) MUKUL JOSHI (SIGN) [Signature] DATE 05/11/00

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| LSI LOGIC - INVENTION DISCLOSURE FORM |   | Disclosure No. P-                    |                                     |
|---------------------------------------|---|--------------------------------------|-------------------------------------|
| D.                                    | WHERE CAN PROTOTYPE BE FOUND?                               |                                      |                                     |
| 5.                                    | TEST OF DEVICE  |                                      |                                     |
| A.                                    | DATE  |                                      |                                     |
| B.                                    | WITNESS   |                                      |                                     |
| C.                                    | RESULT  |                                      |                                     |
| 6.                                    | SALE  |                                      |                                     |
| A.                                    | WAS INVENTION SOLD?   | YES                                  | <input checked="" type="radio"/> NO |
| B.                                    | DATE OF FIRST SALE  |                                      |                                     |
| 7.                                    | USE   |                                      |                                     |
| A.                                    | IS THE INVENTION PRESENTLY BEING USED?                      | YES                                  | <input checked="" type="radio"/> NO |
| B.                                    | ARE THERE SPECIFIC PLANS FOR ITS USE IN THE NEAR FUTURE?    | <input checked="" type="radio"/> YES | NO                                  |
| 8.                                    | RELATED PRINTED PUBLICATIONS, PATENTS, PATENT APPLICATIONS. |                                      |                                     |
| 9.                                    | WAS INVENTION   |                                      |                                     |
| A.                                    | CONCEIVED DURING PERFORMANCE OF GOVERNMENT CONTRACT?        | YES                                  | <input checked="" type="radio"/> NO |
| B.                                    | CONSTRUCTED DURING PERFORMANCE OF GOVERNMENT CONTRACT?      | YES                                  | <input checked="" type="radio"/> NO |
| C.                                    | TESTED DURING PERFORMANCE OF GOVERNMENT CONTRACT?           | YES                                  | <input checked="" type="radio"/> NO |
| D.                                    | CONTRACT NUMBER   |                                      |                                     |
| 10.                                   | WAS INVENTION   |                                      |                                     |
| A.                                    | CONCEIVED DURING PERFORMANCE OF CUSTOMER CONTRACT?          | <input checked="" type="radio"/> YES | NO                                  |
| B.                                    | CONSTRUCTED DURING PERFORMANCE OF CUSTOMER CONTRACT?        | <input checked="" type="radio"/> YES | <input checked="" type="radio"/> NO |
| C.                                    | TESTED DURING PERFORMANCE OF CUSTOMER CONTRACT?             | <input checked="" type="radio"/> YES | <input checked="" type="radio"/> NO |

INVENTORS:

LSI LOGIC

4/28/00  
 4/29/00  
 4/28/00  
 5/1/00  
 05/01/00

Zohar B. Kuten  
 Shmuel Shah

WITNESS, READ AND UNDERSTOOD BY:

(PRINT) Kishor V. Dora (SIGN) [Signature] DATE 5/1/00  
 (PRINT) MUKUL JOSHI (SIGN) [Signature] DATE 05/01/00

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|   |   |                   |
|---|---|-------------------|
| LSI LOGIC - INVENTION DISCLOSURE FORM   |   | Disclosure No. P- |
| D.  | CUSTOMER NAME   | SUN MICROSYSTEMS  |
| <p>THIS DESCRIPTION OF THE INVENTION SHOULD BE WRITTEN IN THE INVENTOR'S OWN WORDS AND GENERALLY SHOULD FOLLOW THE OUTLINE GIVEN BELOW. SKETCHES, PRINTS, PHOTOS AND OTHER ILLUSTRATIONS, AS WELL AS REPORTS OF ANY NATURE IN WHICH THE INVENTION IS REFERRED TO, IF AVAILABLE, SHOULD FORM A PART OF THIS DISCLOSURE AND REFERENCE CAN BE MADE THERETO IN THE DESCRIPTION OF CONSTRUCTION AND OPERATION.</p> |   |                   |
| <p>USE THE ATTACHED SHEETS TO ANSWER THE FOLLOWING QUESTIONS.<br/>(Attach Engineering Reports or other documentation to this form.)</p>   |   |                   |
| 1.  | GENERAL PURPOSE OF THE INVENTION. STATE IN GENERAL TERMS THE OBJECTS OF THE INVENTION.  |                   |
| 2.  | DESCRIBE OLD METHOD(S), IF ANY, OF PERFORMING THE FUNCTION OF THE INVENTION.  |                   |
| 3.  | INDICATE THE DISADVANTAGES OF THE OLD METHOD(S).  |                   |
| 4.  | DESCRIBE THE CONSTRUCTION OF YOUR INVENTION, SHOWING THE CHANGES, ADDITIONS AND IMPROVEMENTS OVER THE OLD METHOD.   |                   |
| 5.  | GIVE DETAILS OF THE OPERATION IF NOT ALREADY DESCRIBED UNDER 4.   |                   |
| 6.  | STATE THE ADVANTAGES OF YOUR INVENTION OVER WHAT HAS BEEN DONE BEFORE.  |                   |
| 7.  | INDICATE ANY ALTERNATE METHOD OF CONSTRUCTION.  |                   |
| 8.  | IF A JOINT INVENTION, INDICATE WHAT CONTRIBUTION WAS MADE BY EACH INVENTOR.   |                   |
| 9.  | FEATURES WHICH ARE BELIEVED TO BE NEW.  |                   |
| 10.   | STATE OPINION OF RELATIVE VALUE OF THE INVENTION.   |                   |
| 11.   | AFTER THE DISCLOSURE IS PREPARED, IT SHOULD BE SIGNED BY THE INVENTOR(S) AND THEN READ AND SIGNED BY TWO WITNESSES IN THE SPACE PROVIDED AT THE BOTTOM OF EACH SHEET. |                   |

INVENTORS:

LSI LOGIC

|   |                           |               |
|---|---------------------------|---------------|
| <p style="text-align: center;"><i>[Signature]</i><br/>Zohar S. Kutler</p> |                           | DATE 4/28/00  |
| <p style="text-align: center;"><i>[Signature]</i><br/>Shimshon Shalev</p> |                           | DATE 4/28/00  |
| WITNESS, READ AND UNDERSTOOD BY:  |                           |               |
| (PRINT) Eishol N. Doren   | (SIGN) <i>[Signature]</i> | DATE 5/1/00   |
| (PRINT) MUKUL JOSHI   | (SIGN) <i>[Signature]</i> | DATE 05/01/00 |

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## LSI LOGIC - INVENTION DISCLOSURE FORM

Disclosure No. P-

## General Purpose :

The general purpose of the invention is to create a robust flip chip package design. Traditional flip chip package design involves the use of 29 mil thick silicon attached to a laminate substrate using eutectic solder bump. This kind of package design has an inherent CTE mismatch between the die (3.5 ppm) and the substrate (16 ppm) and for this reason, an adhesive material (underfill) is used to absorb the stresses on the bump due to the CTE mismatch. However, the use of underfill material has several disadvantages such as poor material adhesion between the underfill and passivation resulting in delamination of the material and subsequent cracking of the solder bumps, difficulty in filling very small gaps (driven by decrease in bump pitch), air bubbles in underfill propagate bump cracks, flux contamination of underfill material causes change in underfill properties and leads to delamination of the underfill layer, etc.

This invention proposes to eliminate CTE mismatch between the substrate and the die by first reducing the thickness of the die and then building several thin film layers of increasing CTE on the die. The thin films would have progressively increasing CTE from the die towards the substrate. This progressive CTE increase would help minimize the CTE mismatch between the individual layers and at the same time would increase the composite CTE of the die-thinfilms to that of the substrate. This increase in the composite CTE of the die-thinfilm reduces the mismatch with the substrate and hence promotes a reliable solder joint with the substrate.

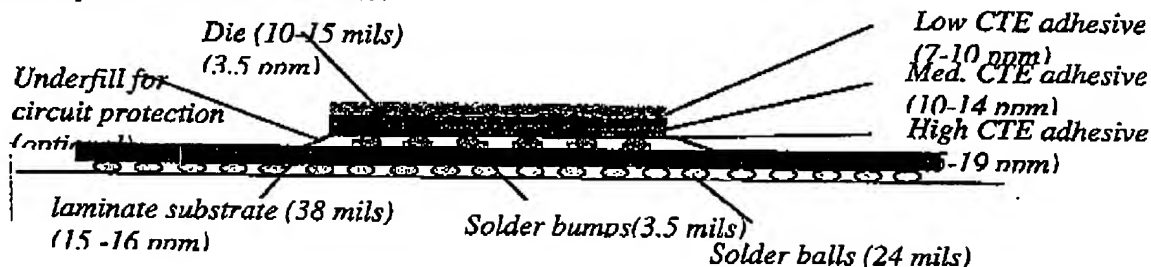


Figure 1: CTE Balanced Flipchip BGA

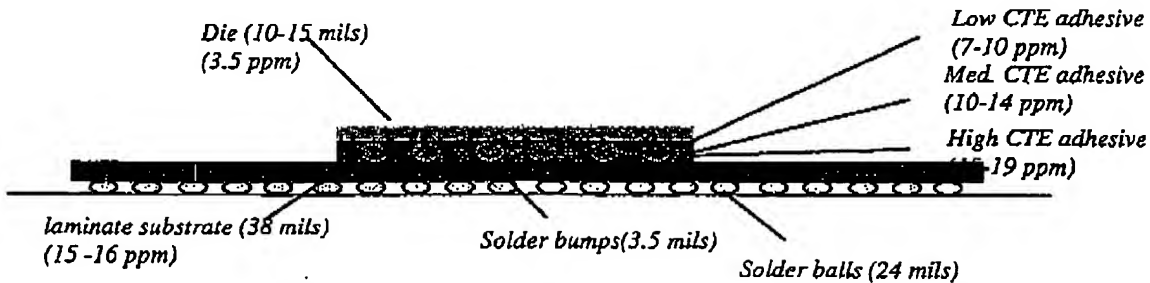
INVENTORS:

LSI LOGIC

|   |                    |               |
|---|--------------------|---------------|
| Zaph S. Kuttan  |                    | DATE 4/28/00  |
| Shrinis Zaval   |                    | DATE 4/29/00  |
| WITNESS, READ AND UNDERSTOOD BY:  |                    |               |
| (PRINT) Kishor V. Desai   | (SIGN) [Signature] | DATE 5/1/00   |
| (PRINT) MUKUL JOSHI   | (SIGN) [Signature] | DATE 05/01/00 |
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## LSI LOGIC - INVENTION DISCLOSURE FORM

Disclosure No. P-



**Figur 2: CTE Balanced Flip Chip BGA – option 2**

In option 2 shown in figure 2, the thin film layers of progressively increasing CTE are used to bond the die to the substrate. This would help minimize the CTE mismatch between the die and the substrate and increase bump fatigue life. In this construction, no underfill material is required.

**Old Construction:**

The old construction shown in figure 2 consists of a chip which is attached to the substrate with an underfill epoxy material filling the gap between the die and the substrate. The substrate and the die warp due to the CTE mismatch between the die and the substrate and the die-underfill interface is under residual stresses due to the CTE mismatch

|   |        |               |  |
|---|--------|---------------|--|
| INVENTORS:  |        |               |  |
|   |        |               |  |
| Zohar S. Kutler   |        | DATE 4/28/00  |  |
|   |        | DATE 4/29/00  |  |
| Shrinani Shew   |        | DATE 4/28/00  |  |
| WITNESS, READ AND UNDERSTOOD BY:  |        |               |  |
| (PRINT) Kishor V. Desai   | (SIGN) | DATE 5/1/00   |  |
| (PRINT) MUKUL JOSHI   | (SIGN) | DATE 05/01/00 |  |
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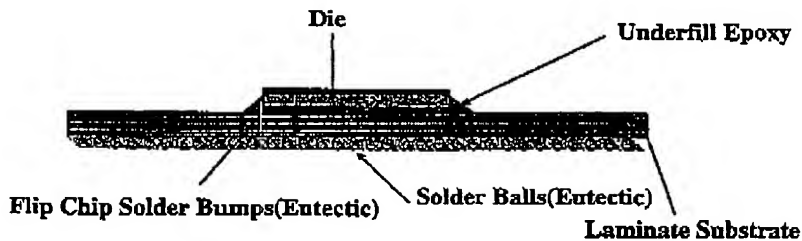


Figure 2: Old construction

**Disadvantages:**

1. Inherent stresses in the package due to CTE mismatch between the die and the substrate
2. Underfill operation is required to absorb the stresses on the solder joints due to CTE mismatch.
3. Underfill adhesion to the die passivation and the solder mask is a concern
4. Underfill voids can potentially cause solder extrusions and shorting of solder bumps.
5. High flip chip bump density is difficult to achieve due to limitation of bump height and underfill gap.
6. For low underfill gaps, the underfill flow is inhibited by flux residues.
7. High flux to underfill volume ratio for low gaps causes die-underfill delamination.

**Advantages of new construction:**

1. Minimal CTE mismatch between the die and substrate
2. Use of underfill is optional for protection of the circuitry
3. Die-underfill/underfill-substrate adhesion is not critical to the functionality of the package
4. The CTE balancing minimizes the thermal stresses in the package and hence increases the package robustness.
5. Very high flip chip bump densities and lower bump pitches can be supported using this package.
6. The number of I/Os on the die could be increased within physical limitations.
7. Very large dies could be soldered on laminate substrates without any solder joint stress issues.

INVENTORS:

LSI LOGIC

|                                  |                           |               |
|----------------------------------|---------------------------|---------------|
| <i>[Signature]</i>               |                           | DATE 4/28/00  |
| Zahid S. Kuteb                   |                           | DATE 4/29/00  |
| <i>[Signature]</i>               |                           | DATE 4/28/00  |
| WITNESS, READ AND UNDERSTOOD BY: |                           |               |
| (PRINT) Vishal V. Desai          | (SIGN) <i>[Signature]</i> | DATE 5/1/00   |
| (PRINT) MUKUL JOSHI              | (SIGN) <i>[Signature]</i> | DATE 05/01/00 |

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## Contribution:


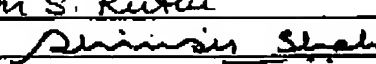
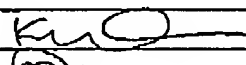
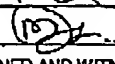
Kumar Nagarajan Ideas  
Zafer Kutlu Ideas  
Shirish Shah Ideas

## Value of the Invention:

The invention would help create a highly reliable flip chip package since the package is balanced in terms of stress

## INVENTORS:

LSI LOGIC

|  |  |               |
|--|--|---------------|
|   |  | 4/28/00       |
| Zafer S. Kutlu   |  | DATE 4/29/00  |
|   |  | DATE 4/28/00  |
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